

STEP 5. Adjusting the Rotation Point

Set the input level to 15 mV, and observe the output on the oscilloscope. Adjust R3—ROTATION PT ADJ CW until the output level just begins to drop, then reverse so that the output is 500 mV. The limiting has now been set to 500 mV.

STEP 6. Adjusting the Compression Ratio

Set the input signal for an output of 500 mV but not in limiting. Note the value (around 15 mV). Next, reduce the input to 1/10 the value noted (around 1.5 mV), for a change of -20 dB. Next, adjust R6—COMP RATIO CW until the output is 160 mV, for an output change of -10 dB. The compression, which is the ratio of output change to input change, in dB, has now been set to 2:1.

STEP 7. Setting the Noise Gate

With the input set at 100 μ V, observe the output on the oscilloscope, and adjust R7—ROT PT SET CCW until the output drops rapidly. “Rock” the control back and forth to find the “knee.” The noise gate has now been set to 100 μ V. The range of the noise gate is from 0.3 mV to over 0.5 mV relative to the output of the buffer. To fit this range to the application, it may be necessary to attenuate the input or apportion the buffer gain and VCA gain differently.

STEP 8. Listening

At this time, it may be desirable to connect an electret microphone to the SSM2166 and listen to the results. Be sure to include the proper power for the microphone’s internal FET (usually +2 V to +5 V dc through a 2.2 k Ω resistor). Experiment with the settings to hear how the results change. Varying the averaging capacitor, C4, changes the attack and decay times, which are best determined empirically. The compression ratio

will keep the output steady over a range of microphone to speaker distance, and the noise gate will keep the background sounds subdued.

STEP 9. Recording Values

With the power removed from the test fixture, measure and record the values of all potentiometers, including any fixed resistance in series with them. If the averaging capacitor, C4, has been changed, note its value, too.

SUMMARY

We have implemented the transfer condition of Figure 2. For inputs below the 100 μ V noise gate threshold, circuit and background noise will be minimized. Above it, the output will increase at a rate of 1 dB for each 2 dB input increase, until the 500 mV rotation point is reached at an input of approximately 15 mV. For higher inputs that would drive the output beyond 500 mV, limiting will occur, and there will be little further increase. The SSM2166 processes the output of the buffer, which in our example is 20 dB, or 10 times the input level. Use the oscilloscope to ensure that the buffer is not being driven into clipping with the highest expected input peaks. Always take the minimum gain in the buffer consistent with the average source level and crest factor (ratio of peak to rms). The wide program range of the SSM2166 makes it useful in many applications other than microphone signal conditioning.

Other Versions

The SSM2165 is an 8-lead version of this microphone preamp with unity buffer gain and preset noise gate threshold. Customized parts are available for large volume users. For further information, contact an ADI sales representative.

SSM2166

Table I. SSM2166 Demo Board Parts List

R1	10 k Ω	Feedback
R2	10 k Ω	Input
R3	50 k Ω Pot	Rotation Point, Adj.
R4	1 k Ω	Rotation Point, Fixed
R5	0 Ω	Comp Ratio, Fixed
R6	100 k Ω Pot	Comp Ratio, Adj.
R7	1 M Ω Pot	Noise Gate, Adj.
R8	1 k Ω	Noise Gate, Fixed
R9	1 k Ω	Gain Adj., Fixed
R10	20 k Ω Pot	Gain Adj.
R11	330 Ω	Mute
R12	100 k Ω	Power Down Pull-Up
C1	0.1 μ F	Input DC Block
C2	1 μ F	Buffer Low f, G = 1
C3	0.1 μ F	+V Bypass
C4	2.2 μ F–22 μ F	Avg. Cap
C5	0.01 μ F	Mute Click Suppress
C6	10 μ F	Coupling
C7	10 μ F	VCA Noise/DC Balance
IC1	SSM2166P	Mic Preamp
IC2	OP113FP	Op Amp, Output Buffer
S1	SPST	Mute
J1	1/8" Mini Phone Plug	MIC Input
J2	RCA Female	Output Jack

SSM2166

Revision History

Location	Page
2/03—Data Sheet changed from REV. A to REV. B.	
Deleted Plastic DIP package	Universal
Change to GENERAL DESCRIPTION	1
Changes to THERMAL CHARACTERISTICS	2
Changes to ORDERING GUIDE	2
Deleted 14-Lead Plastic DIP, OUTLINE DIMENSIONS	15
Updated 14-Lead Narrow-Body SOIC, OUTLINE DIMENSIONS	15

C00357-0-2/03(B)

PRINTED IN U.S.A.